**What is claimed is:**

1. A memory device, comprising:

an array of memory cells arranged in row and columns, each memory cell comprising a select transistor and an electrically programmable resistive element coupled in series therewith, each column of memory cells being coupled to a bit line, each row of memory cells being coupled to a word line, the select transistor in each memory cell having a control terminal coupled to a corresponding word line;

address circuitry for receiving an address value and driving a word line corresponding thereto to a voltage level to activate select transistors of memory cells coupled to the word line corresponding to the address value;

a transistor coupled between a first bit line and a first reference voltage level;

a reference cell coupled to the first bit line, comprising a select transistor and a resistive element coupled in series therewith, the reference cell, the transistor and an addressed memory cell in the column of memory cells coupled to the first bit line forming a differential amplifier circuit; and

control circuitry having an output coupled to a control terminal of the transistor for activating the transistor during a memory read operation.

2. The memory device of claim 1, wherein the electrically programmable resistive element of each memory cell comprises a resistive element having a chalcogenide composition.

3. The memory device of claim 1, wherein the control circuitry deactivates the transistor during a memory write operation.

4. The memory device of claim 1, further comprising write drive circuitry coupled to the first bit line, for placing on the first bit line during a write operation a predetermined voltage level corresponding to a data value, the predetermined voltage level being one of at least two distinct voltage levels.

5. The memory device of claim 4, wherein the write drive circuitry selectively places on the first bit line a second predetermined voltage level between a first voltage level corresponding to a first data value and a second voltage level corresponding to a second data value.

6. The memory device of claim 5, wherein the write drive circuitry places the second predetermined voltage level on the first bit line prior to or at the beginning of a memory write operation.

7. The memory device of claim 1, wherein the memory device executes memory read operations without utilization of a sense amplifier.

8. The memory device of claim 1, wherein the electrically programmable resistive element in each memory cell is programmable to one of at least two distinct resistance values,

and the resistive element in the reference cell has a resistance value between the at least two distinct resistance values.

9. The memory device of claim 1, further comprising a first load element coupled between a second reference voltage level and each memory cell coupled to the first bit line, and a second load element coupled between the second reference voltage level and the reference cell.

10. An electronics device, comprising:

a memory, comprising:

an array of memory cells arranged in rows and columns of memory cells, each memory cell comprising a select transistor and a programmable resistive element coupled in series therewith, each column of memory cells being coupled to a single bit line, each row of memory cells being coupled to a single word line, the select transistor in each memory cell having a control terminal coupled to a corresponding word line;

address circuitry for receiving an address value and driving a word line corresponding thereto to a voltage level to activate select transistors of memory cells coupled to the word line corresponding to the address value;

a transistor coupled between at least one bit line and a reference voltage level;

a reference cell coupled to the at least one bit line, comprising a select transistor and a resistive element coupled in series therewith;

a first load component coupled between a second reference voltage level and the memory cells in the column of memory cells coupled to the at least one bit line;

a second load component coupled between the second reference voltage level and the reference cell, the first and second load components, the reference cell, the transistor and an addressed memory cell in the column of memory cells coupled to the at least one bit line forming a differential amplifier circuit; and

control circuitry having an output coupled to a control terminal of the transistor for activating the transistor during a memory read operation.

11. The electronics device of claim 10, wherein the control circuitry deactivates the transistor during a memory write operation.

12. The electronics device of claim 10, further comprising a processor coupled to address and data terminals of the memory.

13. The electronics device of claim 10, wherein the memory further comprises write circuitry coupled to the control circuitry and the at least one bit line, the write circuitry allowing for any of two or more voltage levels to be applied to the at least one bit line during a write operation, the voltage level applied to the at least one bit line corresponding to a distinct data value and causing a current to flow through the programmable resistive element in the addressed memory cell coupled to the at least one bit line so that the programmable resistive element has a resistance value corresponding to the distinct data value.

14. The electronics device of claim 13, wherein the write circuitry causes a predetermined voltage level to be applied to the at least one bit line prior to or at a beginning of a memory write operation, the predetermined voltage level applied to the at least one bit line being between a first voltage level corresponding to a first data value and a second voltage level corresponding to a second data value.

15. The electronics device of claim 10, further comprising a processing element coupled to the memory.

16. The electronics device of claim 10, wherein the resistive element of the reference cell has a resistance value between a first resistance value corresponding to a first data value and a second resistance value corresponding to a second data value, the memory cells in the memory being capable of storing the first and second data values.

17. The electronics device of claim 10, wherein the programmable resistive element in each memory cell has any of two or more resistance values, depending upon the data value stored in the memory cell.

18. The electronics device of claim 10, wherein a data output terminal of the memory is coupled to the reference cell during a memory read operation.

19. The electronics device of claim 10, wherein the memory comprises a plurality of transistors, each transistor coupled between a distinct bit line and the reference voltage level.

20. The electronics device of claim 10, wherein the memory further comprises a plurality of reference cells, each reference cell coupled to a distinct group of one or more bit lines.

21. The electronics device of claim 10, wherein the memory is free of sense amplifier circuitry.

22. The electronics device of claim 10, wherein the memory executes memory read operations without executing a precharge operations prior thereto.

23. The electronics device of claim 10, wherein the programmable resistive element of each memory cell includes a chalcogenide composition.

24. The electronics device of claim 10, wherein the memory is a phase change memory.

25. A system, comprising:

a memory, comprising:

a memory array of memory cells arranged in rows and columns, each column of memory cells connected to a bit line and each row of memory cells connected to a word line;

a transistor having a first conduction terminal coupled to at least one bit line, a second conduction terminal coupled to a first reference voltage level and a control terminal; and

a reference cell coupled to the at least one bit line, the reference cell, the transistor and an addressed memory cell in the column of memory cells coupled to the at least one bit line forming a differential amplifier circuit having an output signal coupled to a data output terminal of the memory.

26. The system of claim 25, wherein the memory comprises an address input, and the system further comprises a processing unit coupled to the address input and the data output terminal of the memory.

27. The system of claim 25, wherein each of the memory cells in the memory array comprises an electrically programmable resistive element and a select transistor coupled thereto, a control terminal of the select transistor being coupled to a corresponding bit line.

28. The system of claim 27, wherein the electrically programmable resistive element comprises a chalcogenide resistive element.

29. The system of claim 27, wherein the reference cell comprises a resistive element and a transistor coupled thereto, the resistive element of the reference cell having a resistance value between a first resistance value corresponding to a first logic value and a second resistance value corresponding to a second logic value.

30. The system of claim 27, further comprising a write drive circuit having an output coupled to the at least one bit line, the write drive circuit controlling a voltage on the at least one

bit line during a memory write operation so that the electrically programmable resistive element in an addressed memory cell is subject to a current of a predetermined amount, the predetermined amount corresponding to a data value to be stored in the addressed memory cell.

31. The system of claim 25, further comprising a control circuit having an output coupled to a control terminal of the transistor, the control circuit activating the transistor during a memory read operation and deactivating the transistor during a memory write operation.

32. An integrated circuit, comprising:

a plurality of memory cells, each memory cell coupled to a data line;

a reference cell coupled to the data line;

a transistor coupled between the data line and a reference voltage; and

a circuit for selecting one memory cell at a time, wherein the selected memory cell, the reference cell, and the transistor form a differential amplifier circuit.

33. The integrated circuit of claim 32, wherein each memory cell comprises a resistive element having a chalcogenide composition.

34. The integrated circuit of claim 32, wherein each memory cell includes a programmable resistive element.

35. The integrated circuit of claim 32, wherein the memory cells form part of a phase change memory.